REMARKS

In the present Office Action, claims 1-21 were pending before the Office. Of these, claims 1, 7, 13, and 17 were the only independent claims. The Office Action rejected claims 1-21.

The specification was objected to. Claims 1-12 were objected to. Claims 1-12 were rejected under 35 U.S.C. § 112, first paragraph. Claims 1-21 were rejected under 35 U.S.C. § 112, first paragraph. Claims 1-12 were rejected under 35 U.S.C. § 112, second paragraph. Claims 1-12 were rejected under 35 U.S.C. § 101. Claims 1-21 were rejected under 35 U.S.C. § 102. For at least the reasons set forth herein, the objections/rejections are traversed and reconsideration is respectfully requested.

Claims 1 and 7 have been amended. No claims have been added, cancelled, or withdrawn.

A. OBJECTION TO THE SPECIFICATION AND REJECTION UNDER 35 U.S.C. § 112, FIRST PARAGRAPH

Claims 1-12 were rejected under 35 U.S.C. § 112, first paragraph. On page 5 of the Office Action, the Examiner again asserts that "selecting a bit" as recited in the instant claims is not described in the specification sufficiently to enable one of ordinary skill in the art. The Examiner appears to suggest that if Applicants' arguments are valid, that this limitation is rendered obvious.

Applicants respectfully submit that Applicants' arguments are valid, but that the point of Applicants' arguments may have been misconstrued as going beyond arguing that those of ordinary skill in the art have known how to "select a bit" since at lest 1946. Since those of ordinary skill in the art know how to "select a bit," then the description is enabling since it describes the method as including "selecting a bit" from a memory array of an integrated circuit (IC). Thus, the rejection of claims 1-12 as not being enabled can be withdrawn since the feature of "selecting a bit" in the context of a method for testing an IC is enabled. Similarly, the objection to the specification can be withdrawn. Applicant also respectfully submits that even assuming *arguendo* this particular feature is obvious, the combination of known elements can be a novel and non-obvious combination. Thus, since the prior art does not disclose or suggest Applicants' particular manner of selecting a bit from a memory array during an ABIST test of an IC and storing the selected bit, Applicants' claims are allowable over the prior art of record.

Claims 1-21 stand rejected under 35 U.S.C. § 112, first paragraph, as not being enabled, or including new matter, with respect to the feature, "wherein an outcome of the ABIST test is determined based on the stored selected bit," added by amendment to claims 1, 7, 13, and 17. The Examiner alleges that

"There is no description in the application as originally file [sic] to suggest what kind of effect if any the stored selected bit has on the ABIST test." Applicants respectfully traverse this rejection and this allegation, submit that much of the specification is written in the context of ABIST testing, and direct the Examiner's attention to page 13 the specification, where it is stated that:

> As mentioned above, in at least one embodiment, the initial state value of the output of the multiplexer 404 (e.g., the initial value of the ABIST dot output line 408) is of a high logic state (e.g., via pull-up circuitry). Accordingly, if the bit output via the global dot line 318 of the first memory array 210 has a high logic state, the gate of the first NFET N1 will be low, the first NFET N1 will be off, and the ABIST dot line 408 will remain in its initial state (e.g., high). Alternatively, if the bit output via the global dot line 318 of the first memory array 210 has a low logic state, the gate of the first NFET N1 will be high, the first NFET N1 will turn on, and the ABIST dot line 218 will be pulled low via the first and second NFETs N1, N2. Bits of the other memory arrays may be similarly output to the ABIST dot line 408. In this manner, the output signal of the multiplexer 404 will match the selected input data signal (e.g., the bit selected from one of the memory arrays in step 504) of the multiplexer 404 for the selected one of the plurality of memory arrays 210-216.

This clearly provides support for and an enabling description of the feature added by amendment to claims 1, 7, 13, and 17. Thus, the feature added to the claims is not new matter and the description is fully enabling of this feature to one of ordinary skill in the art. The rejection can therefore

be withdrawn.

B. OBJECTION TO CLAIMS 1-12

The Examiner has objected to claims 1-12 as not including "testing an IC circuit" in their main bodies. Applicants respectfully submit that independent claims 1 and 7 as previously presented provided limitations such as "during an ABIST test" and "an outcome of the ABIST test" that provide positive recitations of testing an IC circuit in the bodies of the claims. Since claims 2-6 and 8-12 depend from independent claims 1 and 7, they also include these positive recitations. To expedite prosecution, Applicants have amended claim 7 to include the positive recitation of "during an ABIST test" in its body. Claims 1 and 7 thus clearly provide positive recitation of testing an IC circuit in their bodies, claims 2-6 and 8-12 depending therefrom incorporate such positive recitations, and the objection can be withdrawn.

C. REJECTION UNDER 35 U.S.C. § 112, SECOND PARAGRAPH

Claims 1-12 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. The Examiner takes issue with the usage of "selecting a bit," alleging that it is not clear whether the phrase refers to the same bit in dependent claims vs. the independent claim in which the phrase first appears. Applicant respectfully submits that in each dependent

claim, the phrase is actually "wherein selecting a bit from each of a plurality of memory arrays includes" which clearly refers to the step in independent claim 1 of "selecting a bit during an ABIST test from each of a plurality of memory arrays," and in claim 7 of "selecting a bit from each of a plurality of memory arrays." It is the step to which the phrase refers, not the bit. Thus, the claims are clear and the rejection can be withdrawn.

D. REJECTION UNDER 35 U.S.C. § 101

Claims 1-12 stand rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. Specifically, claims 1 and 7 were rejected as reciting an abstract idea without any tangible results. Arguments were presented in the previous response regarding the tangibility of selecting and storing a bit. These arguments are reiterated, but to expedite prosecution, Applicants have added specific recitations in claims 1 and 7 to indicate that the memory arrays from which the bit is selected are part of the integrated circuit being tested, and that the selected bit is stored in a component of the integrated circuit. Support for these changes is found throughout the specification and thus the changes are not new matter. Since changes are wrought to a component of the IC chip, the method produces a tangible effect, claims 1 and 7 are statutory, and the rejection under 35 U.S.C. § 101 can be withdrawn.

E. REJECTION UNDER 35 U.S.C. § 102(e)

Claims 1-21 again stand rejected under 35 U.S.C. § 102(e) as being anticipated by Jain (U.S. Patent No. 6,853,597). The Examiner states that Jain discloses a method and apparatus for an IC having a BIST control unit for testing a plurality of memory banks simultaneously that anticipates claims 1, 7, 13, and 17. Applicants respectfully again traverse this rejection.

The Examiner rebuts Applicants' arguments against Jain by stating that the selected faulty bit BitF from the final test results TR to the BIST control unit generated by the comparator unit 106, as disclosed by Jain, corresponds to the claimed selected bit from the memory since the comparator unit is a species of the genus "memory array" comprising the memory bank 104 and the comparator unit and as such anticipates Applicants' selected bit. The Examiner therefore concludes that Applicants' claims do not distinguish between a bit selected from a memory unit and a bit selected from a comparator unit since both the memory bank and the comparator are formed on the IC chip 100 of Jain.

The Examiner appears to be arguing that each comparator/memory bank pair disclosed in Jain is equivalent to the memory array of the instant invention. Applicants do not understand how the Examiner can reach this conclusion when a

comparator simply outputs a result of a comparison between two signals. As such, a comparator hardly qualifies as a memory bank or even a memory cell since there is no storage of data *per se*. Even if one were to accede to this categorization of the comparator/memory bank pairs, the limitations of, for example, instant claim 1 require selecting a bit from each memory array, selecting one of the memory arrays, and storing the selected bit of the selected memory array are not disclosed by Jain since there is no selection in Applicants' particular manner as between the comparator output and the memory bank contents during the BIST.

Applicants respectfully submit that Jain does not and can not select "a bit from each of a plurality of memory arrays formed on an IC chip," select "one of the plurality of memory arrays," and store "the selected bit from the selected memory array." Assuming for the sake of argument that Jain's memory bank is the equivalent of one of the instant memory arrays, Applicants' invention overcomes the prior art practice, such as that shown in Jain, of having separate comparators for each memory bank, thus saving chip real estate. Jain clearly states that a separate comparator is connected to each of a plurality of memory banks and to the source of the test pattern, there thus being a number of comparators equal to the number of Jain's memory banks.

To illustrate the distinctiveness of Applicants'

claimed invention, Applicants' invention could be applied to that of Jain to reduce the number of comparators employed by having a plurality of memory banks connected to a single comparator, "selecting a bit from each of" the memory banks, a memory bank to be tested being selected by Applicants' "selecting one of a plurality of memory arrays." However, this is not what Jain does. There is no selection of a memory array in Jain as is required by, for example, Applicants' claim 1 because Jain uses a discrete comparator for each memory bank, testing the content of the respective memory bank against a test pattern. Because of the one-to-one memory bank/comparator relationship in Jain, there is no way that Jain can select a bit from each memory bank and select a memory bank as would be required, for example, by instant claim 1. Thus, since Jain does not disclose all of the limitations of, for example, instant claim 1, the rejection of claims 1-21 as being anticipated by Jain can be withdrawn and the claims can be allowed.

F. CONCLUSION

Since the Applicants assert that all the independent claims as amended are in condition for allowance and all remaining claims properly depend from the independent claims, Applicants assert that all claims are allowable.

Applicants do not believe a Request for Extension of Time is required but if it is, please accept this paragraph as a Request for Extension of Time and authorization to charge the requisite extension fee to Deposit Account No. 04-1696.

Applicants do not believe any additional fees are due regarding this Amendment. However, if any additional fees are required, please charge Deposit Account No. 04-1696.

Respectfully Submitted,

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